REMARKS

The Examiner has rejected Claims 1-29 under 35 U.S.C. 102(e) as being anticipated by Migdal et al. (PN 6,426,753), hereinafter "Migdal." Applicant respectfully disagrees with this assertion.

In particular, the Examiner has relied on Migdal to show applicant's claimed "sending an instruction request to memory utilizing a texture module in a graphics pipeline" and "receiving instructions from the memory in response to the instruction request utilizing the texture module in the graphics pipeline."

> "Accordingly, the present invention provides a cache memory for high latency and out-of-order return of texture data. The present invention includes a texture cache memory that is capable of working efficiently in computer systems where there is a long latency from the time the texture data is requested and the time the texture data is available for use. In addition, the present invention is capable of handling texture responses which enter into the texture cache memory in a different order from which they were requested. The present invention significantly improves performance of a computer system having a distributed texture memory architecture." (col. 3, lines 20-32)

Applicant emphasizes that such passage merely mentions the conventional fetching of "texture data." In sharp contrast, applicant teaches and claims sending "instructions requests" and retrieving "instructions" "utilizing a texture module." By retrieving the instructions utilizing the texture module, much pipeline bandwidth is saved at the input of the texture module, since prior art configuration data at least in part need not necessarily be received from the rasterizer. Moreover, the memory traditionally employs a high-bandwidth connection with the texture module, which may be used for efficient retrieval of the instructions.

The instructions may then be used by the texture module in order to control various graphics processing involving the texels, pixels, and/or primitives, etc. For example, the instructions may control how subsequent texels may be mapped to pixels associated with primitives. Moreover, the instructions may be used to control

the mapping, or blending, of the texels with the pixels, in accordance with the instructions. Simply nowhere in the prior art is there such a combination of features for fulfilling the foregoing objectives.

To further emphasize such advantages, applicant claims in dependent claims that "the instructions are adapted for controlling a texture environment module coupled to the texture module" (see Claim 6). The Examiner relies on col. 5, lines 15-20 of Migdal to show such feature in the prior art.

> "The G chip 105 accepts instructions and data from Crosstalk streams 106. The instructions are executed by microprocessor 103 and G chip 105. G chip 105 also performs geometric calculations on vertex data. Data is temporarily cached in SRAM 104. Eventually, the resulting vertex data is sent over the high bandwidth network 102 to one of the R subsystems." (col. 5, lines 15-20)

After a careful review, applicant contends that such excerpt is lacking, especially in view of the shortcomings of the Examiner's application of Migdal to the independent claims. For example, the abovementioned "microprocessor" and "G chip" do not include a "texture module," a claimed by applicant. Only applicant teaches and claims sending "instructions requests" and retrieving "instructions" "utilizing a texture module" which provides the aforementioned advantages that are non-existent in the prior art including Migdal.

Similarly, applicant claims that "the initial instructions control at least the sending of the instruction request by the texture module" (see Claim 9), "a complete instruction set is received in response to the instruction request" (see Claim 18), and "a partial instruction set is received in response to the instruction request" (see Claim 19).

All of the pending independent claims are thus deemed allowable along with any claims depending therefrom. A specific prior art showing of such claim limitations or a notice of allowance is respectfully requested.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. For payment of any fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP064/P000286).

Respectfully submitted,

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